

<b>Notic of References Cited</b>	Application/Control No. 09/536,927	Applicant(s)/Patent Under Reexamination HAWRYLUK ET AL.	
	Examiner Toniae M. Thomas	Art Unit 2822	Page 1 of 1

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	B	US-4,402,762 B1	09-1983	JOHN et al.	438/482
	C	US-5,399,506 B1	03-1995	TSUKAMOTO	438/301
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	M	US-			

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**NON-PATENT DOCUMENTS**

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	U	Wolf, "Isolation Technologies for Integrated Circuits," Silicon Processing for the VLSI Era - Vol. 2: Process Integration, Lattice Press, 1990, pp.66-78.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.